Attorney Reference B0301T

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(Nonsigning Inventor)

As a below named officer, I hereby declare that:

Sole Inventor: Katsuhiko Sasahara
Residence: Tokyo, Japan
Citizenship: Japanese
Post Office Address: Famile Square Kokubunji 1004,
1-14 Kokubunji-Honcho 4-chome,
Tokyo 185-0012, Japan

I believe he is the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD OF SETTING INPUT PIN CAPACITY

the specification of which was filed on October 2, 2003, as United States Application Number 10/676,071.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) of a foreign application for patent listed below.

Prior Foreign Application: 2002-293148
County: Japan
Filed (Day/Month/Year): 07/10/2002

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and the such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named officer, I hereby appoint the following agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Yusuke Takeuchi (Reg.No.30,921), Manabu Kanesaka (Reg.No.31,467), and
Satoru Takeuchi (Reg.No.53,670)

Send Correspondence to: Yusuke Takeuchi
TAKEUCHI & TAKEUCHI
1700 Diagonal Rd., Suite 310
Alexandria, VA 22314

Direct Telephone Calls to: Yusuke Takeuchi (703) 684-9777

Signed: _____ Date: _____

Name: Fumitaka Yokoyama

Title: General Manager of Oki Electric Industry Co., Ltd.

ATTACHMENT 5

(Translation of Attachment 3)

To: Katsuhiko Sasahara

Date: November 26, 2003

From: Oki Electric Industry Co., Ltd.
Intellectual Property Section
10-3 Shibaura 4-chome
Minatoku, Tokyo
Japan

REQUEST FOR INVENTOR'S SIGNATURE
Our Ref. F-01ED0647-US-ED

Dear Sir:

A patent application for the invention made by you and described in Japanese Patent Application No. 2002-293148 was filed in the United States.

Please sign and answer the attached documents according to the following instruction. Since there is a due date to file with the US Patent Office, please return the signed documents by December 8, 2003.

The documents to be signed are Declaration, Assignment, and Confidentiality Agreement. Please understand the contents of these documents and sign them at the marked positions. Please see the attached papers "Checking documents/Signing in English" for signing Declaration and Assignment. Please return all the documents.

Attachments:

(1) Confidentiality Agreement one copy
(2) Declaration and Assignment one copy
(3) English Specification with claims and drawings one copy
(4) "Request for Inventor's Signature" Checking documents/Signing in English one copy

ATTACHMENT 6

(Translation of Attachment 4)

OKI INVENTION/DESIGN REPORT
(Confidential)

Received No. 01 ED 0647

Received Date: 29/??/2002

Title of Invention: Semiconductor Memory Device

Summary of Invention: Method of setting an input pin capacity in a common chip mounted on a single chip package and multi-chip package

No. of Inventors: one

Assignment: I hereby attest that the right to receive a utility or design patent in Japan and foreign countries for the invention or design described above is assigned to Oki Electric Industry Co., Ltd. in terms and conditions of "Office Regulations."

Signed by: Katsuhiko Sasahara in Japanese and English
Section: SiSC Memory Design

Joint Inventors: none

Joint Applicants: none

Obligations to Others: none

Test Model: none

Application Deadline: none

Use: DRAM

Prior Art: Not searched

Related Report: none